PATENT ABSTRACTS OF JAPAN

(11)Publication number : 07-336651

(43)Date of publication of application : 22.12.1995

(51)Int.Cl. H04N 7/01
H04N 7/24

(21)Application number : 06-154280

(22)Date of filing : 13.06.1994

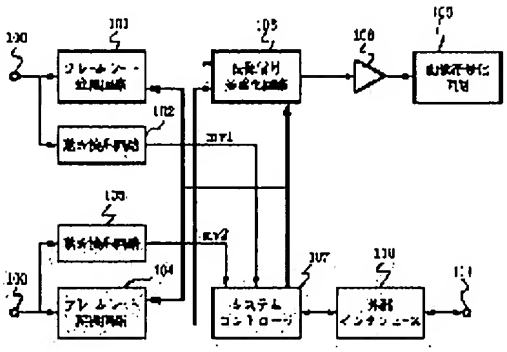
(71)Applicant : CANON INC

(72)Inventor : TAKAYAMA TADASHI

(54) VIDEO PROCESSOR

(57)Abstract:

PURPOSE: To easily eliminate redundant signal components when multiplexed video signals are compressed and transmitted by converting the frame rate of video signals inputted from a video signal input means.



CONSTITUTION: In the composite video signal inputted via video signal input terminals 100 and 103, the frame rates by appearances are reduced by each of frame rate conversion circuits 101 and 104 in accordance with the frame extraction ratio (frame rate conversion ratio) which is preliminarily set within the frame rate conversion circuits 101 and 104 by a system controller 107. In this case, all the video signals of each inputted frame are not transmitted to a video signal multiplexing circuit 1 06 and the only video signals of the frames extracted at fixed space of 1/2, 1/3 or 1/4 are outputted as video signals for multiplexing. The signals are multiplexed by a video signal multiplexing circuit 106 and are transmitted via a buffer amplifier 108 and a moving image encoding circuit 109.

LEGAL STATUS

[Date of request for examination]

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rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

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CLAIMS

[Claim(s)]
[Claim 1] The image processor characterized by having a frame rate conversion means to be the image processor which has two or more video-signal input means and a video-signal multiplexing means to multiplex two or more video signals inputted from the video-signal input means concerned, and to change the frame rate of the video signal inputted from said video-signal input means.
[Claim 2] It is the image processor which has two or more video-signal input means and a video-signal multiplexing means to multiplex two or more video signals inputted from the video-signal input means concerned. A frame rate conversion means to change a frame rate by supplying the video signal of the frame extracted at fixed spacing out of the video signal of each frame inputted from said video-signal input means to said video-signal multiplexing means, The image processor characterized by having a setting-out means to set up frame extractability to this frame rate conversion means.
[Claim 3] Said frame rate conversion means is claim 1 characterized by being prepared for said two or more video-signal input means of every, or an image processor according to claim 2.
[Claim 4] Said setting-out means is an image processor according to claim 2 characterized by being prepared for said two or more video-signal input means of every.
[Claim 5] Said setting-out means is an image processor according to claim 2 characterized by setting up frame extractability according to the amount of motions of the image which has a motion detection means to detect the amount of motions of an image, and was detected by this motion detection means.
[Claim 6] Said setting-out means is an image processor according to claim 2 characterized by setting up the frame extractability specified with the instruction from an external device.
[Claim 7] Said setting-out means is an image processor according to claim 2 characterized by setting up the frame extractability which has an input means to input frame extractability and was inputted by this input means.
[Claim 8] The image processor characterized by having a field rate conversion means to be the image processor which has two or more video-signal input means and a video-signal multiplexing means to multiplex two or more video signals inputted from the video-signal input means concerned, and to change the field rate of the video signal inputted from said video-signal input means.
[Claim 9] It is the image processor which has two or more video-signal input means and a video-signal multiplexing means to multiplex two or more video signals inputted from the video-signal input means concerned. A field rate conversion means to change a field rate by supplying the video signal of the field extracted at fixed spacing out of the video signal of each field inputted from said video-signal input means to said video-signal multiplexing means, The image processor characterized by having a setting-out means to set up field extractability to this field rate conversion means.
[Claim 10] Said field rate conversion means is claim 8 characterized by being prepared for said two or more video-signal input means of every, or an image processor according to claim 9.
[Claim 11] Said setting-out means is an image processor according to claim 9 characterized by being prepared for said two or more video-signal input means of every.
[Claim 12] Said setting-out means is an image processor according to claim 9 characterized by setting

up field extractability according to the amount of motions of the image which has a motion detection means to detect the amount of motions of an image, and was detected by this motion detection means.
[Claim 13] Said setting-out means is an image processor according to claim 9 characterized by setting up the field extractability specified with the instruction from an external device.
[Claim 14] Said setting-out means is an image processor according to claim 9 characterized by setting up the field extractability which has an input means to input field extractability and was inputted by this input means.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the suitable image processor for the remote monitoring system and the video conference system which use the transmission line of a low bit rate especially about the image processor which superimposes two or more video signals and generates a multi-image.
[0002]
[Description of the Prior Art] Conventionally, a video signal as shown in drawing 5 (a) and (b) is inputted, respectively, and this kind of equipment is outputting the video signal which superimposed the video signal of drawing 5 (a) and (b) as shown in drawing 5 (c) from the image output terminal.
[0003]
[Problem(s) to be Solved by the Invention] However, with the above-mentioned conventional configuration, since both two input video signals on which it was superimposed serve as a dynamic image of the same frame rate, in case the video signal after superposition is compressed by codecs, such as a video conference system and remote monitoring system, and is transmitted, also when one image input signal is not not much important, it is compressed and transmitted to the image input signal and EQC of another side.
[0004] Moreover, in the method which improves the compressibility of a dynamic image by motion vector which is represented by advice H.261 of ITU-TS, since a redundant compression signal was temporarily generated by change of the video signal in the noise and the image part which is not not much important of a video-signal processor etc. even when there are few motions of a photographic subject, the transmission band was tight with those signals, and there was a problem that the quality of a total video signal deteriorated.
[0005] This invention was made under such a background and the object is in enabling it to remove simply the redundant signal component generated in case the multiplexed video signal is compressed and transmitted.
[0006]
[Means for Solving the Problem] In order to attain the above-mentioned object, invention according to claim 1 is an image processor which has two or more video-signal input means and a video-signal multiplexing means to multiplex two or more video signals inputted from the video-signal input means concerned, and has a frame rate conversion means to change the frame rate of the video signal inputted from said video-signal input means.
[0007] In order to attain the above-mentioned object, invention according to claim 2 It is the image processor which has two or more video-signal input means and a video-signal multiplexing means to multiplex two or more video signals inputted from the video-signal input means concerned. A frame rate conversion means to change a frame rate by supplying the video signal of the frame extracted at fixed spacing out of the video signal of each frame inputted from said video-signal input means to said video-signal multiplexing means, It has a setting-out means to set up frame extractability to this frame rate conversion means.

[0008] In order to attain the above-mentioned object, in invention according to claim 3, said frame rate conversion means in claim 1 or claim 2 is established for said two or more video-signal input means of every.
[0009] In order to attain the above-mentioned object, in invention according to claim 4, said setting-out means in claim 2 is established for said two or more video-signal input means of every.
[0010] In order to attain the above-mentioned object, said setting-out means in claim 2 has a motion detection means to detect the amount of motions of an image, and it consists of invention according to claim 5 so that frame extractability may be set up according to the amount of motions of the image detected by this motion detection means.
[0011] In order to attain the above-mentioned object, said setting-out means in claim 2 consists of invention according to claim 6 so that the frame extractability specified with the instruction from an external device may be set up.
[0012] In order to attain the above-mentioned object, said setting-out means in claim 2 has an input means to input frame extractability, and it consists of invention according to claim 7 so that the frame extractability inputted by this input means may be set up.
[0013] In order to attain the above-mentioned object, invention according to claim 8 is an image processor which has two or more video-signal input means and a video-signal multiplexing means to multiplex two or more video signals inputted from the video-signal input means concerned, and has a field rate conversion means to change the field rate of the video signal inputted from said video-signal input means.
[0014] In order to attain the above-mentioned object, invention according to claim 9 It is the image processor which has two or more video-signal input means and a video-signal multiplexing means to multiplex two or more video signals inputted from the video-signal input means concerned. A field rate conversion means to change a field rate by supplying the video signal of the field extracted at fixed spacing out of the video signal of each field inputted from said video-signal input means to said video-signal multiplexing means, It has a setting-out means to set up field extractability to this field rate conversion means.
[0015] In order to attain the above-mentioned object, in invention according to claim 10, said field rate conversion means in claim 8 or claim 9 is established for said two or more video-signal input means of every.
[0016] In order to attain the above-mentioned object, in invention according to claim 11, said setting-out means in claim 9 is established for said two or more video-signal input means of every.
[0017] In order to attain the above-mentioned object, said setting-out means in claim 9 has a motion detection means to detect the amount of motions of an image, and it consists of invention according to claim 12 so that field extractability may be set up according to the amount of motions of the image detected by this motion detection means.
[0018] In order to attain the above-mentioned object, said setting-out means in claim 9 consists of invention according to claim 13 so that the field extractability specified with the instruction from an external device may be set up.
[0019] In order to attain the above-mentioned object, said setting-out means in claim 9 has an input means to input field extractability, and it consists of invention according to claim 14 so that the field extractability inputted by this input means may be set up.
[0020]
[Function] In invention according to claim 1, said frame rate conversion means removes simply the redundant signal component generated in case the multiplexed video signal is compressed and transmitted by changing the frame rate of the video signal inputted from said video-signal input means.
[0021] The redundant signal component which generates in case the video signal which multiplexed when a frame rate changes when said frame rate conversion means supplies the video signal of the frame extracted at fixed spacing out of the video signal of each frame inputted from said video-signal input means to said video-signal multiplexing means, and said setting-out means sets up frame extractability to said frame rate conversion means compresses in invention according to claim 2 and it transmits

removes simply.
[0022] Said frame rate conversion means established for said two or more video-signal input means of every in invention according to claim 3 removes simply the redundant signal component generated in case the multiplexed video signal is compressed and transmitted by changing a frame rate to the video signal inputted from a video-signal input means to correspond.
[0023] Said setting-out means established for said two or more video-signal input means of every in invention according to claim 4 removes simply the redundant signal component generated in case the multiplexed video signal is compressed and transmitted by setting up frame extractability to the video signal (said frame rate conversion means) inputted from a video-signal input means to correspond.
[0024] In invention according to claim 5, said setting-out means removes simply the redundant signal component generated in case the multiplexed video signal is compressed and transmitted by setting up frame extractability according to the amount of motions of the image detected by said motion detection means.
[0025] In invention according to claim 6, said setting-out means removes simply the redundant signal component generated in case the multiplexed video signal is compressed and transmitted by setting up the frame extractability specified with the instruction from an external device.
[0026] In invention according to claim 7, said setting-out means removes simply the redundant signal component generated in case the multiplexed video signal is compressed and transmitted by setting up the frame extractability inputted by said input means.
[0027] In invention according to claim 8, said field rate conversion means removes simply the redundant signal component generated in case the multiplexed video signal is compressed and transmitted by changing the field rate of the video signal inputted from said video-signal input means.
[0028] In invention according to claim 9 said field rate conversion means A field rate is changed by supplying the video signal of the field extracted at fixed spacing out of the video signal of each field inputted from said video-signal input means to said video-signal multiplexing means. Said setting-out means removes simply the redundant signal component generated in case the multiplexed video signal is compressed and transmitted by setting up field extractability to said field rate conversion means.
[0029] Said field rate conversion means established for said two or more video-signal input means of every in invention according to claim 10 removes simply the redundant signal component generated in case the multiplexed video signal is compressed and transmitted by changing a field rate to the video signal inputted from a video-signal input means to correspond.
[0030] Said setting-out means established for said two or more video-signal input means of every in invention according to claim 11 removes simply the redundant signal component generated in case the multiplexed video signal is compressed and transmitted by setting up field extractability to the video signal (said field rate conversion means) inputted from a video-signal input means to correspond.
[0031] In invention according to claim 12, said setting-out means removes simply the redundant signal component generated in case the multiplexed video signal is compressed and transmitted by setting up field extractability according to the amount of motions of the image detected by said motion detection means.
[0032] In invention according to claim 13, said setting-out means removes simply the redundant signal component generated in case the multiplexed video signal is compressed and transmitted by setting up the field extractability specified with the instruction from an external device.
[0033] In invention according to claim 14, said setting-out means removes simply the redundant signal component generated in case the multiplexed video signal is compressed and transmitted by setting up the field extractability inputted by said input means.
[0034]
[Example] Hereafter, one example of this invention is explained, referring to a drawing.
[0035] Drawing 1 is the block diagram showing the outline configuration of the image processor by one example of this invention. In addition, this image processor is applied to remote monitoring system or a video conference system.
[0036] In drawing 1 , it is the motion detector which detects the amount of motions of the video signal

which 100,103 was connected to the video-signal input terminal, 101,104 was connected to the video-signal input terminal 100,103, respectively, and the frame rate conversion circuit which changes and outputs the frame rate on the appearance of the video signal inputted into each terminal, and 102,105 were connected to the video-signal input terminal 100,103, respectively, and was inputted into each terminal.

[0037] In addition, it is constituted so that frame rate conversion may be performed by outputting selectively the video signal of the frame extracted at fixed spacing out of the video signal of each inputted frame, but the frame rate conversion circuit 101,104 of this example can carry out the operation hand of this invention, not only this but when raising a frame rate by repeating and outputting the video signal of each frame depending on the case.

[0038] 106 makes an input signal the output video signal of the frame rate conversion circuit 101,104. The video-signal multiplexing circuit which generates and outputs the video signal which multiplexed them, Buffer amplifier for 108 to output the video signal generated by the video-signal multiplexing circuit to external devices, such as a codec, 109 an input video signal For example, the circuit which carries out dynamic-image coding, for example, the image coding network encoded in advice H.261 of ITU-TS, An interface circuitry for the system controller with which 107 controls the whole equipment, and 110 to connect an external device with a system controller 107, and 111 are the connectors connected to the interface circuitry 110. In addition, a system controller 107 is constituted by CPU, ROM, RAM, etc., and CPU performs various control, such as setting out of the frame extractability in the frame rate conversion circuit 101,104, as a work area using RAM according to the program by which presetting was carried out to ROM.

[0039] Drawing 2 is the block diagram showing the detailed configuration of the frame rate conversion circuit 101,104 in drawing 1 . In drawing 2 , the inside of a dotted line shows the frame rate conversion circuit 101,104 in drawing 1 . It is the A/D converter which the buffer amplifier by which 201 was connected to the video-signal input terminal 100,103, the clamping circuit which 202 is connected to the output side of the buffer amplifier 201, and reproduces the dc component of an input video signal, and 203 are connected to the output side of a clamping circuit 202, and the low pass filter for removing the clinch signal in the case of sampling and 204 are connected to the output side of a low pass filter 203, and changes an analog video signal into a digital signal.

[0040] The synchronizing separator circuit which buffer amplifier for a Video RAM to connect an input side to A/D converter 204, connect an output side to D/A converter 213, respectively, and for 212 accumulate the digitized video signal, the low pass filter by which 214 was connected to the output side of D/A converter 213, and 215 to send out the output side of a low pass filter 214 to the video-signal multiplexer 106, and 205 are connected to the output side of the buffer amplifier 201, and separates the synchronizing signal component of an input video signal, and 206 are the oscillators for write control circuit 207.

[0041] The write control circuit which 207 makes a reference signal the synchronizing signal separated by the synchronizing separator circuit 205, and generates the write-in signal to Video RAM 212, 208 makes an input signal the synchronizing signal separated by the synchronizing separator circuit 205. The write-in timing signal generating circuit which generates the write-in gate signal (timing signal) to Video RAM 212 with the period set up by the control signal (a0, a1) from a system controller 107, The AND gate which controls the write-in signal to Video RAM 212 by which 209 was generated by the write control circuit 207 by the gate signal generated by the write-in timing signal generating circuit 208, The read-out control circuit which 211 makes a reference signal the synchronizing signal separated by the synchronizing separator circuit 205, and generates the read-out signal from Video RAM 212, and 210 are the oscillators for read-out control circuit 211.

[0042] Next, if actuation by this whole video-signal multiplexer is explained, in drawing 1 , the composite video signal inputted through the video-signal input terminal 100,103 will be seen by the frame rate conversion circuit 101,104 according to the frame extractability (frame rate conversion rate) beforehand set up in the frame rate conversion circuit 101,104 by the system controller 107, respectively, and the upper frame rate will be reduced.

[0043] Although the frame rate conversion circuit 101,104 has the delay circuit of the video signal using a Video RAM inside although mentioned later for details, and read-out from the Video RAM concerned is performed by the same frame rate as the HARASHIN number, the frame rate on appearance is reduced to 1/2, 1/3, or 1/4 by writing in two frames of the HARASHIN number once at once, three frames, or four frames. Without sending out all the video signals of each inputted frame to the video-signal multiplexer 106, if it puts in another way, the video signal only of the video signal of the frame extracted at fixed spacing of 1/2, 1/3, or 1/4 is carried out for multiplexing, and it is outputted.
[0044] The composite video signal with which it was inputted through the video-signal input terminal 100,103, and saw as mentioned above, and the upper frame rate was reduced is multiplexed by the video-signal multiplexing circuit 106, and is sent out via the buffer amplifier 108 and a connector 109 to an external device.
[0045] Moreover, it is inputted also into the motion detector 102,105, respectively, the amounts mv1 and mv2 of motions of each video signal are measured, and the composite video signal inputted through the video-signal input terminal 100,103 is notified to a system controller 107. Although explanation is omitted about a motion detector, it is based on a technique well-known [inter-frame correlation etc.]. A system controller 107 investigates the value of the amounts mv1 and mv2 of motions of each video signal measured in the motion detector 102,105, and changes the frame extractability (frame rate conversion rate) in the frame rate conversion circuit 101,105 dynamically also during actuation by comparing each value with the boundary value set up beforehand.
[0046] Moreover, a system controller 107 sends out the value of the amounts mv1 and mv2 of motions of each video signal measured in the current extractability or the current motion detectors 102 and 105 of the frame rate conversion circuit 101,104 to external devices, such as a computer apparatus and a codec, via the external-interface circuit 110 and a connector 111. Under the present circumstances, if there is an instruction from external devices, such as other television conference terminals, each frame extractability of the frame rate conversion circuit 101,104 will be set as the value specified with an instruction.
[0047] Next, the setting-operation of frame extractability is explained according to the flow chart of drawing 4 . in addition, a motion is so large that C10, C11, C12, C13 and C14 which are mentioned later, and C20, C21, C22, C23 and C24 are constants which show the amount of motions beforehand set up on the program and a value is large -- being shown -- **** -- C10 -- < -- C11 -- < -- C12 -- < -- C13 -- < -- C14 and C20 -- < -- C21 -- < -- C22 -- < -- C23 -- < -- it is C24.
[0048] A system controller 107 initializes M and N (M and N are "0" or "1"), respectively to the control signals a0 and a1 for frame extractability setting out (step S1). And read-out (step S2) and the amount mv1 of motions of a video signal are measured with the set points C10, C11, C12, and C13 for the amounts mv1 and mv2 of motions of the video signal detected by the motion detector 102,105 (step S3).

[0049] Consequently, if it is C10 <=mv1<C11, it will be referred to as control signal a0=1 and a1=1 that frame extractability of the frame rate conversion circuit 101 should be made one fourth (step S4). If it is C11 <=mv1<C12, it will be referred to as control signal a0=0 and a1=1 that frame extractability of the frame rate conversion circuit 101 should be made one third (step S5). If it is C12 <=mv1<C13, it will be referred to as control signal a0=1 and a1=0 that frame extractability of the frame rate conversion circuit 101 should be made one half (step S6). If it is C13 <=mv1<C14, it will be referred to as control signal a0=0 and a1=0 that frame extractability of the frame rate conversion circuit 101 should be made 1/1 (step S7).
[0050] Next, the amount mv2 of motions of a video signal is measured with the set points C20, C21, C22, C23, and C24 (step S8).
[0051] Consequently, if it is C20 <=mv2<C21, it will be referred to as control signal a0=1 and a1=1 that frame extractability of the frame rate conversion circuit 104 should be made one fourth (step S9). If it is C21 <=mv2<C22, it will be referred to as control signal a0=0 and a1=1 that frame extractability of the frame rate conversion circuit 104 should be made one third (step S10). If it is C22 <=mv2<C23, it will be referred to as control signal a0=1 and a1=0 that frame extractability of the frame rate conversion

circuit 104 should be made one half (step S11). If it is C23 <=mv2<C24, it will be referred to as control signal a0=0 and a1=0 that frame extractability of the frame rate conversion circuit 104 should be made 1/1 (step S12). And return and the same frame extractability setting-out processing are repeated to step S2.

[0052] The more there are few amounts of motions of a video signal so that clearly from the above explanation, the more he is trying to set up small frame extractability. Thus, even if the video signal with few motions does not prepare a special transmission mode or compress mode in the image coding network 109 by making frame extractability small, it becomes able [a motion] to remove simply the redundant signal component generated by the codec in the multiplexing field of few video signals.

[0053] Next, actuation of a frame rate conversion circuit is explained.

[0054] In drawing 2 , the video signal inputted from the video-signal input terminal 100 or 103 is led to a clamping circuit 202 and a synchronizing separator circuit 205 via a buffer circuit 201. After the video signal which went via the clamping circuit 202 has a high frequency component removed by the clearance filter 203 by return, it is written in by the write-in signal WR2 which it is changed into a digital signal with A/D converter 204, and is later mentioned to Video RAM 212.

[0055] In a synchronizing separator circuit 205, Horizontal Synchronizing signal HD and Vertical Synchronizing signal VD are extracted from an input video signal, and the write control circuit 207 and the read-out control circuit 211 are supplied. Vertical Synchronizing signal VD is supplied also to the gate signal generating circuit 208. In the write control circuit 207, the basic clock WR for writing to Video RAM 212 which carried out phase simulation to Horizontal Synchronizing signal HD supplied from the synchronizing separator circuit 205 and Vertical Synchronizing signal VD is generated. The basic clock RD for read-out from Video RAM 212 which similarly carried out phase simulation to Horizontal Synchronizing signal HD supplied from the synchronizing separator circuit 205 also in the read-out control circuit 211 and Vertical Synchronizing signal VD is generated.

[0056] Gate signal WR.gate is generated according to the frame extractability set up by the combination of each value of the control lines a0 and a1 with the system controller 107 in the gate signal generating circuit 208. Gate signal WR.gate is used in order to carry out ON/OFF of the basic clock WR for the writing generated by the write control circuit 207. After the basic clock WR for the writing generated by gate signal WR.gate generated in the gate signal generating circuit 208 and the write control circuit 207 has an AND taken in the AND gate 209, it is supplied to Video RAM 212 as a write-in signal WR2 with the final output of the AND gate 209.

[0057] On the other hand, the basic clock RD for read-out generated by the read-out control circuit 211 is used for read-out as it is from Video RAM 212. After an unnecessary high frequency component is removed and the video signal read from Video RAM 212 goes via a buffer 215 with the low pass filter 214 after being changed into the analog signal by D/A converter 213, it is led to the latter buffer amplifier 108.

[0058] An above child is shown in the timing chart of drawing 3 . In addition, in drawing 3 , the upward-slant-to-the-right hatching part of a thick wire shows the period when the read-out signal RD from Video RAM 212 is active, the lower right of a thin line shows the period when the basic clock WR for writing to Video RAM 212 is active, and, as for the ** hatching part, the lower right of a thick wire shows the period when the write-in signal WR2 to Video RAM 212 is active, as for the ** hatching part.

[0059] In drawing 3 , Signals VD and HD are the Vertical Synchronizing signals and Horizontal Synchronizing signals which were generated by the synchronizing separator circuit 205, respectively. Although signal ODD/EVEN is not specified by the block diagram, it is the field distinction signal of the input video signal generated in the interior of the write-in timing signal generating circuit 208 from aforementioned Vertical Synchronizing signal VD and aforementioned Horizontal Synchronizing signal HD. When signal ODD/EVEN is "1", the odd number field is shown, and in the case of "0", the even number field is shown. Signal WR.gate generates a pulse as shown in drawing 3 with the combination of each value of the control signals a0 and a1 for frame extractability setting out supplied from a system controller 107. Since the circuit for pulse generation is easily realizable with a well-known technique,

explanation has not been given. In drawing 3 , the write-in signal WR2 to Video RAM 212 is supplied [the period of "1"] for signal WR.gate.

[0060] Therefore, as shown in drawing 3 , in the case of a0=0 and a1=0, the frame rate of the video signal written in Video RAM 212 and the video signal read from Video RAM 212 becomes equal, and frame extractability becomes 1/1. In the case of a0=1 and a1=0, the video signal written in Video RAM 212 is set to one half of the frame rates of the video signal read from Video RAM 212, frame extractability is set to one half, it sees, and the upper frame rate is reduced. Similarly, in the case of a0=0 and a1=1, in the case of a0=1 and a1=1, the video signal written in Video RAM 212 is set to one fourth of the frame rates of the video signal read from Video RAM 212 (frame extractability is 1/4) by setting the video signal written in Video RAM 212 to one third of the frame rates of the video signal read from Video RAM 212 (frame extractability being 1/3).

[0061] In addition, it cannot be overemphasized that this invention is applicable for example, also not only about the video-signal multiplexer of 2 inputs but the video-signal multiplexer of 3 or more ****s, without limiting this invention to the above-mentioned example. Moreover, the signal aspect may be the discrete signal of RGB also about a frame rate converter, and you may be the gestalt of brightness and a color-difference signal. Furthermore, the frame extractability in a frame rate converter does not need to be limited to the range indicated by the above explanation.

[0062] Moreover, to the video-signal input terminal for dynamic images with many motions, a frame rate conversion circuit and a motion detector are not prepared, but a frame rate conversion circuit and a motion detector can also prepare a frame rate conversion circuit and a motion detector only to the video-signal input terminal a dynamic image with few motions, and for static images, when it turns out beforehand that a dynamic image with many motions, a dynamic image with few motions, a static image, etc. are inputted respectively for example, without preparing for every video-signal input terminal.

[0063] Furthermore, without setting up frame extractability (frame rate) according to the amount of motions of the video signal detected by the motion detector, input means, such as a key switch for setting up frame extractability, for example, are established, and you may make it set up frame extractability small with this input means about the video signal which the user judged not to be important, for example. Moreover, although frame extractability was set up according to the amount of motions of a video signal, you may make it this invention set up frame extractability in the above-mentioned example according to the entropy of not only this but a video signal, for example, the amount of a high frequency component. Or frame extractability may be set up according to image size. What is necessary is in short, just to change frame extractability according to the amount of information of a video signal.

[0064] Moreover, it is also possible to prepare a field rate conversion circuit instead of a frame rate converter especially in the case of the video signal scanned sequentially instead of interlace scanning.

[0065]

[Effect of the Invention] As explained above, according to this invention, in the image processor which has a means to multiplex two or more input video signals, the redundant signal component generated in case compression transmission of the video signal after multiplexing is carried out is easily removable by establishing the frame rate conversion means for reducing a frame rate or a field rate at least, or a field rate conversion means. When this equipment is applied as an input unit of the television conference which uses the transmission line of a low bit rate especially, or monitoring system, the large improvement in the image quality of a transmission image can be expected.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the outline configuration of the image processor by one example of this invention.
[Drawing 2] It is the block diagram showing the configuration of a frame rate conversion circuit.
[Drawing 3] It is the timing diagram which shows actuation of a frame rate conversion circuit.
[Drawing 4] it is the flow chart which shows the setting-operation of a frame rate conversion rate (frame extractability) -- it comes out.
[Drawing 5] It is drawing showing the example of an input video signal and an output video signal.
[Description of Notations]
100,103 -- Video-signal input terminal
101,104 -- Frame rate conversion circuit
102,105 -- Motion detector
106 -- Video-signal multiplexing circuit
107 -- System controller
109 -- Image coding network
110 -- External interface
205 -- Synchronizing separator circuit
207 -- Write control circuit
208 -- Write-in timing signal generating circuit
209 -- AND gate
212 -- Video RAM

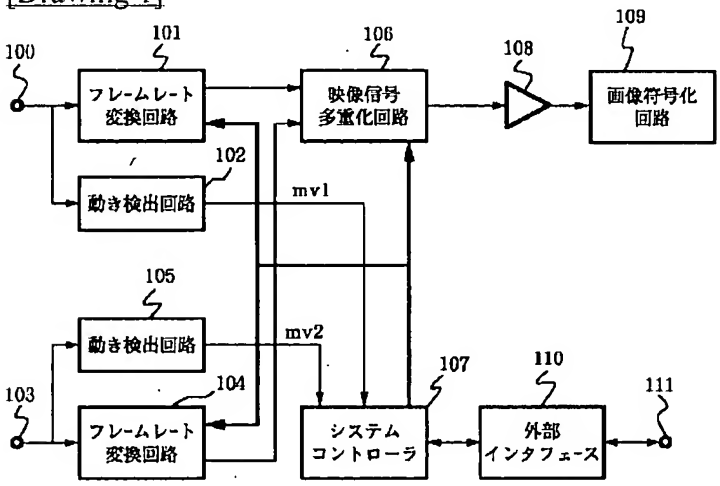
[Translation done.]

* NOTICES *

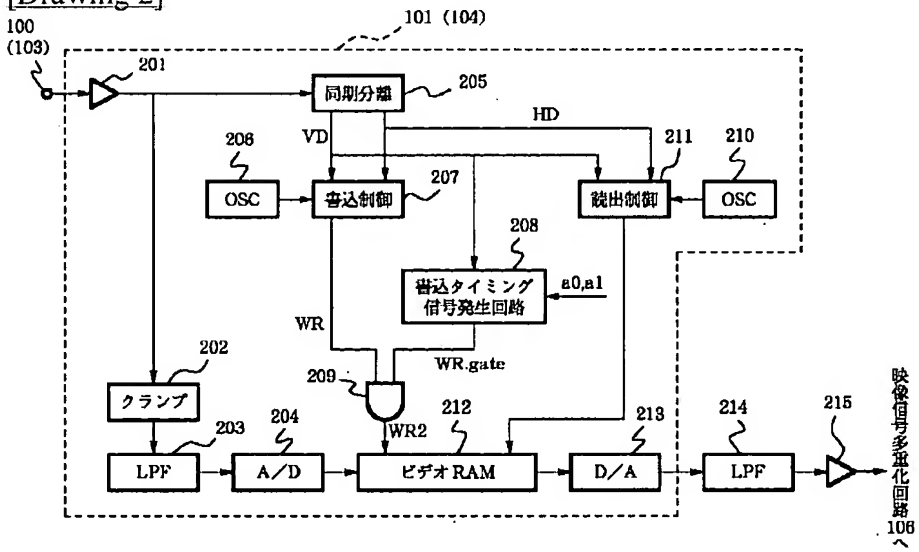
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

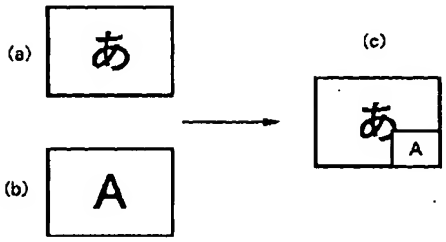
[Drawing 1]



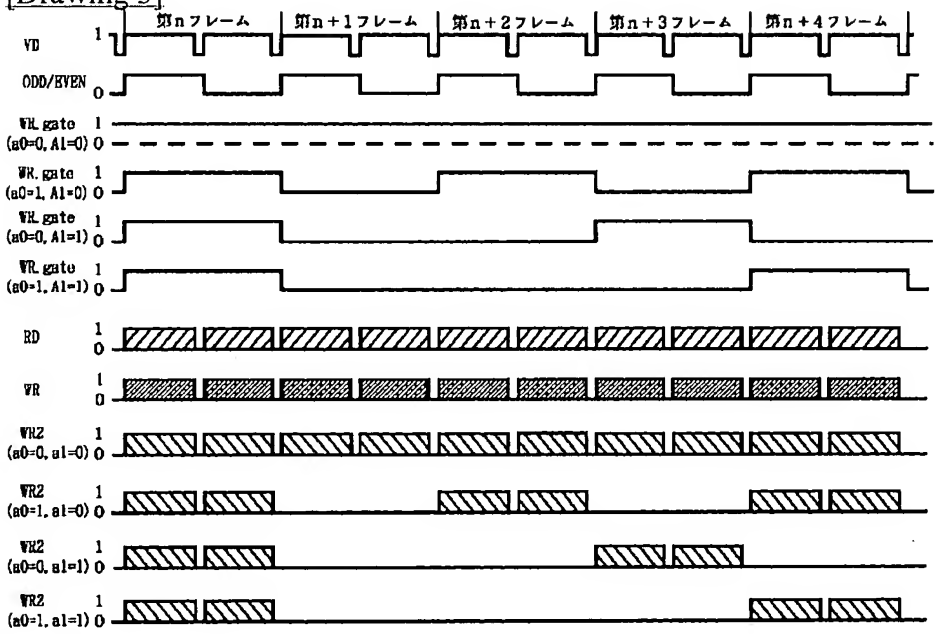
[Drawing 2]



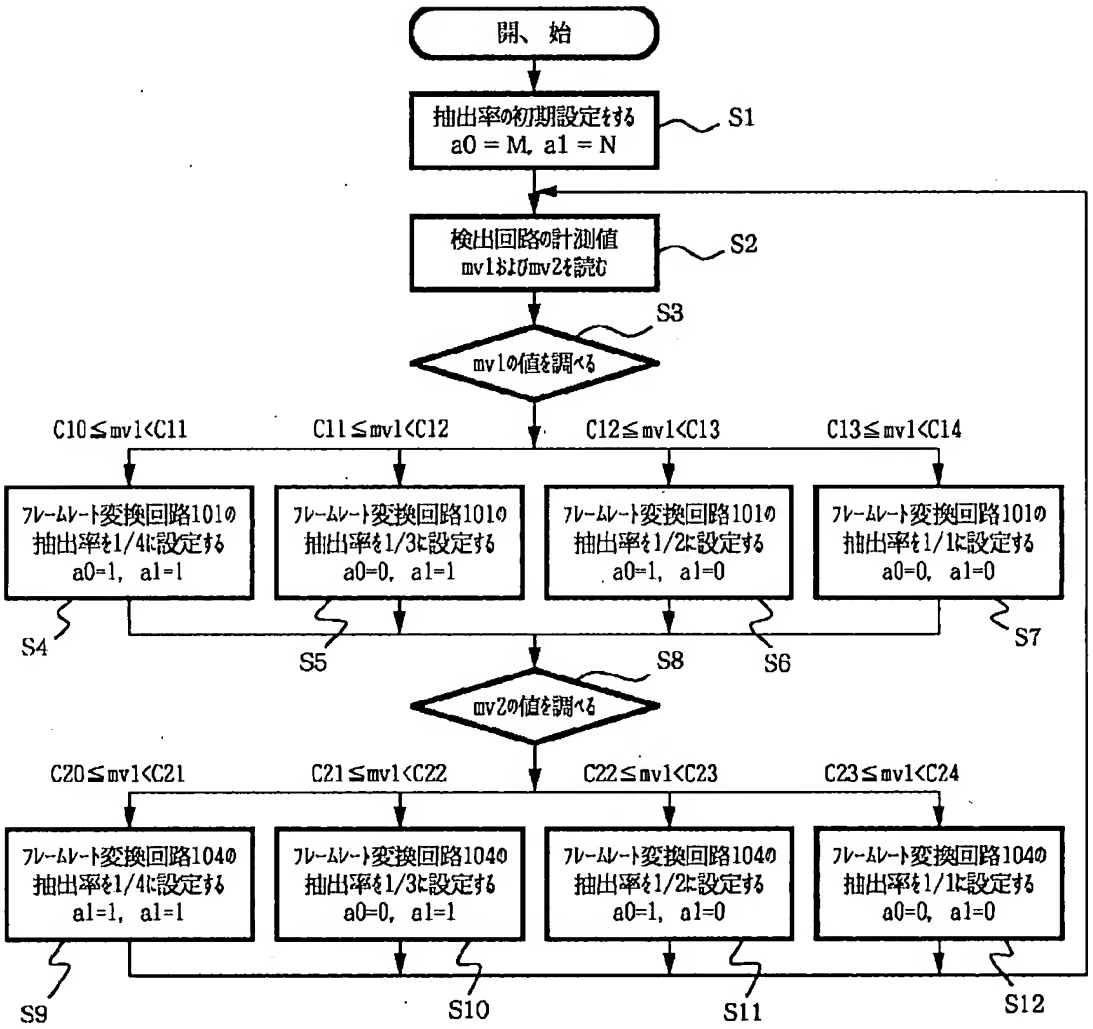
[Drawing 5]



[Drawing 3]



[Drawing 4]



[Translation done.]